National Institute of Technology Karnataka, Surathkal

TTTC India - VLSI Test Workshop - Mangalore Session

MARCH 30, 2019

ABOUT SYMPOSIUM

Verification and testing are the key steps in VLSI chip design cycle to ascertain their functional correctness and defect free fabrication. VLSI testing encompasses all spectrums of test methods and structures embedded in IC design to ensure the quality of manufactured devices. The test methods typically include fault modelling, test generation and fault simulation. The test structures often employ design for testability (DFT) techniques, such as scan design and built-in self-test (BIST).

SCOPE

This symposium focuses on providing participants with basic understanding of the most recent DFT advances in logic, memory, delay and SOC testing as well as mixed signal IC testing. The talks cover wide ranging topics in the following fields from basics to advanced level :

- **Evolution of Design for test**
- **Cell Aware Test / Defect Oriented Test**
- **Small Delay Defect Testing**
- **Emerging Automotive Electronic Industry & Associated Test Challenges**
- **IEEE 1687: IJTAG**

The symposium is open to students, faculty and working professionals with basic knowledge of VLSI Design.

LHC – C, NITK SURATHKAL
9:30AM – 5:30PM

RESOURCE PERSONS

Prakash Narayanan is a Sr.Technical Lead, Member Group Technical Staff at Texas Instruments India Pvt. Ltd., responsible for leading the DFT efforts for several projects at TI ranging from wireless microcontroller SOCs to the most recent mmWave Radar SOCs being developed at TI. He has several granted patents in logic and memory test with several more filed. He has co-authored conference papers at ITC, VTS, DATE, and IOLTS apart from many papers at EDA vendor conferences and TI internal over the years.

Wilson Pradeep is a Lead DFT Engineer with Texas Instruments, Bangalore. He has over 10 years of experience in DFT and digital front end design. He is currently working as DFT lead for various Industrial and Automotive Radar SoC platform designs. Wilson has authored regular papers in premier test conferences like ITC, ATS and VTS apart from major EDA and TI internal conferences and has several patents covering DFT innovations.

Abhishek Chaudhary - Abhishek Chaudhary is Manager, DFT Engineering at Rambus Bangalore. He has over 11 years of experience in DFT. He and his team are responsible for end to end DFT for all high speed SERDES and Memory PHY IPs across Rambus worldwide. He has also worked on DFT for automotive chips at Freescale Semiconductor (Now NXP) in the past. He holds patents and has published papers in reputed IEEE conferences and symposiums in India and abroad.

Registration is free and is limited to 70 with first come first basis.
Registration Link: bit.ly/vlsi_symposium

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